arXiv:2507.05523v1 [cs.ET] 7 Jul 2025

Adaptive Variation-Resilient Random Number Generator for Embedded Encryption

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(Dated: July 9, 2025)

With a growing interest in securing user data within the internet-of-things (IoT), embedded encryption has become of paramount importance, requiring light-weight high-quality Random Number Generators (RNGs). Emerging stochastic device technologies produce random numbers from stochastic physical processes at high quality, however, their generated random number streams are adversely affected by process and supply voltage variations, which can lead to bias in the generated streams. In this work, we present an adaptive variation-resilient RNG capable of extracting unbiased encryption-grade random number streams from physically driven entropy sources, for embedded cryptography applications. As a proof of concept, we employ a stochastic magnetic tunnel junction (sMTJ) device as an entropy source. The impact of variations in the sMTJ is mitigated by employing an adaptive digitizer with an adaptive voltage reference that dynamically tracks any stochastic signal drift or deviation, leading to unbiased random bit stream generation. The generated unbiased bit streams, due to their higher entropy, then only need to undergo simplified post-processing. Statistical randomness tests based on the National Institute of Standards and Technology (NIST) test suite are conducted on bit streams obtained using simulations and FPGA entropy source emulation experiments, validating encryption-grade randomness at a significantly reduced hardware cost, and across a wide range of process-induced device variations and supply voltage fluctuations.

I. INTRODUCTION

Demand for hardware security is growing rapidly due to the unprecedented growth of the Internet of Things (IoT) [1]. Data encryption is becoming more important, with a drive to move it towards the device side and away from the cloud. This move provides higher levels of security; however, it imposes stringent size and energy constraints on the hardware. These constraints are also coupled with stringent requirements for encryption quality, imposing a challenging design trade-off between hardware compactness and encryption quality [2].

For cryptographic applications, the encryption key is the main secret necessary for data decryption, since it is assumed that adversaries are aware of the encryption algorithm used [3–5]. Therefore, it is crucial to generate keys through random processes that make them unlikely to be guessed. Such procedures are implemented using subsystems known as Random Number Generators (RNGs), and are of two categories: True-RNGs (TRNGs) and Pseudo-RNGs (PRNGs). The latter include circuits that implement mathematical or computational algorithms that are typically used to generate random sequences; however, such sequences are deterministic and can be regenerated if the initial 'seed' is known, making them susceptible to prediction penetration. On the other hand, TRNGs are circuits that produce random bits based on physically random phenomena in emerging device technologies, making them more reliable for applications where security is of great concern [6, 7], such as

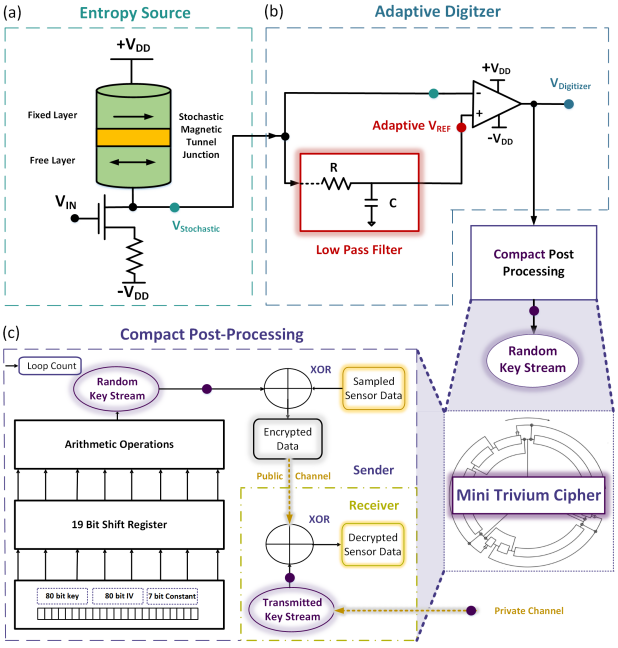

FIG. 1. Block Diagram of the adaptive RNG comprising (a) an entropy source (sMTJ here), (b) an adaptive digitizer with a low-pass-filter generated moving reference voltage, and (c) compact post processing.

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wireless communication [8, 9] and remote sensing [10–13].

Hardware TRNG implementations are based on the utilization of devices with unique properties or the exploitation of intrinsic noise present in classical electronic devices. TRNGs have become essential for cryptography-related IoT applications, as well as for probabilistic computing [14–17]. The challenge in using TRNGs is that they are adversely affected by variations in the fabrication process of the device technology used [18], leading to bias in generated bit streams. Moreover, in IoT devices, which are mainly battery powered, fluctuations in the supply voltage can also adversely affect TRNGs [19, 20].

In this work, we present an adaptive RNG that extracts high-quality unbiased random bit streams from a time-varying stochastic signal obtained from an entropy source. The system is primarily designed for bit steam extraction from a true-random entropy source, such as a stochastic Magnetic Tunnel Junction (sMTJ), shown in Fig. 1 (a), but we will also show that it can still perform satisfactorily well with a pseudo-random source, such a Linear Feedback Shift Register (LFSR). The complete block diagram of the proposed system is shown in Fig. 1. In our proposed adaptive RNG, an adaptive digitizer is employed to eliminate any bias, enhancing the resilience of the system to process-induced and supply-voltage variations in true-random entropy sources, and enhancing the randomness qualities of pseudo-random entropy sources.

Due to the enhanced randomness qualities of the generated bitstreams, we show that light-weight post-processing is sufficient for acceptable encryption-grade randomness, allowing further savings in hardware. This is demonstrated using both a conventional Trivium cipher [21–23], shown in Fig. 2 (b), and a simplified more compact version of it, the Mini-Trivium, shown in Fig. 2 (d). Schematic illustrations of a conventional and the proposed adaptive RNG are depicted in Fig. 2.

Section II discusses entropy sources, Sec. III presents an adaptive TRNG with a true-random sMTJ entropy source and Sec. IV presents an adaptive RNG with a pseudo-random LFSR entropy source with experimental implementation. Finally, Sec. V concludes the paper.

II. THE ENTROPY SOURCE

Entropy sources are a core component in RNGs, as they provide the source of randomness. Deterministic PRNGs employ pseudo-random digital sources in the form of shift registers and are regarded as RNGs with low-quality randomness. On the other hand, TRNGs based on conventional complementary-metal-oxide-semiconductor (CMOS) technology commonly employ noise in devices, such as thermal noise [24] or random telegraph noise (RTN) [25], as their physical entropy source and generally require oscillator circuits. Moreover, CMOS-based TRNGs need intricate extraction and complex post-processing circuits to mitigate output correlation and bias. Additionally, they are also highly affected by variations in process, voltage, and temperature (PVT) [26], necessitating entropy-tracking feedback loops [27].

Emerging devices utilizing stochastic switching mechanisms, like magnetic switching [28], resistive switching [29], and phase change [30], have been proposed as promising entropy sources for TRNGs due to their inherent stochastic nature. Notably, devices with stochastic temporal dynamics driven by fluctuations in thermal energy, such as stochastic magnetic tunnel junctions (sMTJs) [31, 32], do not require voltage pulsing or forced switching mechanisms to trigger their stochastic response, making them excellent entropy sources for TRNGs. However, as stated earlier, a major challenge in these device technologies is their limited resilience to process-induced and supply voltage variations.

In order to demonstrate the utility of our adaptive RNG, we test it with an sMTJ as a true-random source and an LFSR as a pseudo-random source. The first is investigated in Sec. III and the latter is implemented and validated experimentally in Sec. IV.

A. Stochastic MTJ Model

Prior to presenting our design for an sMTJ-based adaptive TRNG, in order to be able to study the system's behavior when employing an sMTJ entropy source, a model for the sMTJ is needed. This is achieved by a two-fold process. First, the sMTJ resistance fluctuations are simulated using MATLAB, and the resulting sMTJ behavior is fed into SPICE as a variable resistor with time-varying conductance.

The dynamics of the stochastic switching of the sMTJ are controlled by the fluctuations of the magnetization state (m_z(t)) of the free magnet layer, that fluctuates from 1 to -1 continuously, where 1 refers to a parallel state in reference to the fixed magnet layer, while -1 is an antiparallel state, as shown in Fig. 2 (a). These fluctuations give rise to an sMTJ whose time-varying conductance ($G(t)$) is defined as:

$$G(t) = G_0\left[1 + m_z(t)\frac{TMR}{2+TMR}\right] \tag{1}$$

where G_0 is the average conductance, and TMR is the tunneling magnetoresistance ratio. The TMR depends on the ratio between the parallel (R_P) and the antiparallel (R_{AP}) resistance states of the sMTJ and is defined as:

$$TMR = \frac{R_{AP} - R_P}{R_P} \tag{2}$$

MATLAB is used to emulate the sMTJ's dynamic magnetization state m_z(t) and its probability distribution. The resultant m_z(t) vector is then used in solving eq.

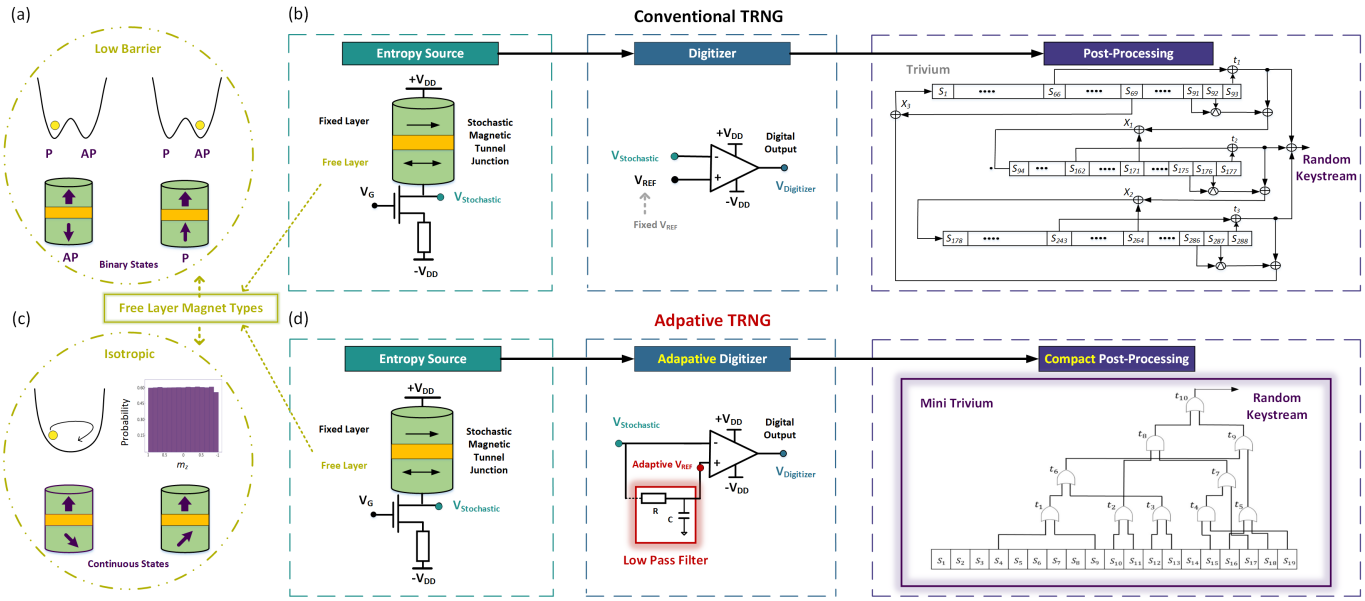

FIG. 2. Comparison between conventional TRNGs and the proposed adaptive TRNG. Illustration of magnetization dynamics in stochastic MTJs for (a) low-barrier magnets and (c) isotropic magnets. The uniform probability distribution of the magnetization in the vertical z-direction (m_z(t)) depicts characteristics of isotropic sMTJs (inset of (c)). Schematic block diagram Illustration of (b) a conventional TRNG system and (d) the proposed adaptive TRNG system with the adaptive digitizer and the Mini Trivium compact post-processing blocks.

(1) to obtain the time-varying vector $G(t)$, which is received by SPICE software as a time-varying resistance according to $G(t)$.

Fig. 2 (a) illustrates the switching mechanism of the sMTJ device employing a low barrier free magnet layer, having two stable magnetic configurations: parallel (P) and antiparallel (AP) states. In our analysis, we have employed an isotropic magnet for the free layer, owing to its uniform m_z(t) distribution as depicted in Fig. 2 (c), which makes it a favorable entropy source due to the higher degrees of freedom offered by the isotropic free layer magnet [33].

III. ADAPTIVE TRNG WITH A TRUE-RANDOM ENTROPY SOURCE

This section presents an example TRNG design based on the adaptive RNG concept, by employing the s-MTJ true-random entropy source discussed in Sec. II. After the entropy source, the two remaining components of the adaptive TRNG system are: (1) the adaptive digitizer and (2) the post-processing circuit. These are presented in subsections A and B, respectively, followed by simulation results and variation-resilience analysis in subsections C and D, respectively.

A. Adaptive Digitizer

Once a stochastic signal is generated by the entropy source, the signal needs to be converted from analog to digital, and this is the role of the digitizer. This is usually done by comparing the analog stochastic voltage signal with a reference analog voltage (V_{REF}) using a comparator that converts voltages above V_{REF} to high output voltages (ideally V_{DD}: a digital 1) and voltages below V_{REF} to low output voltages (ideally GND: a digital 0). Ideally, the desired output of the digitizer would be a random bit stream that is 50 % ones (1's) and 50 % zeros (0's) on average. Based on this, V_{REF} is a critical design parameter. In our design, instead of applying a fixed V_{REF} to the comparator, we design a low-pass filter (LPF) circuit that generates an adaptive moving V_{REF} from the stochastic signal ($V_{stochastic}$) corresponding to its short-term average, as shown in Fig. 3 (d). This V_{REF} adapts to changes in the stochastic signal, such as voltage drift or mismatch from the designed-for voltage levels due to process-induced or supply voltage variations.

The LPF is typically implemented using a resistor (R) and a capacitor (C) in a simple RC LPF configuration, as shown in Fig. 2 (d). The time constant τ_{LPF} of the RC circuit determines how quickly the reference voltage adapts to changes in $V_{stochastic}$, and is expressed as follows:

$$\tau_{LPF} = RC \tag{3}$$

where R and C are the resistance and capacitance of the

resistor and capacitor in the RC circuit respectively. The cutoff frequency f_{LPF} of the LPF is given by:

$$f_{LPF} = \frac{1}{2\pi RC} \tag{4}$$

The selection of R and C depends on how fast the system needs to adapt to fluctuations in $V_{stochastic}$. In a system employing an sMTJ entropy source, f_{LPF} needs to be much lower than the average fluctuation frequency f_c of the sMTJ, which can be characterized using the correlation time of magnetization in the sMTJ (τ_c) [33]. This requires the following inequality to be satisfied:

$$\tau_{LPF} > \tau_c \tag{5}$$

Careful design of the sMTJ can allow τ_c to be across a wide range of timescales from nano-seconds [34] to milli-seconds [31], accommodating the needs of different applications, as τ_c has an impact on the final throughput of the RNG.

B. Post-Processing Circuit: The Trivium Cipher

After the adaptive digitizer, post-processing is needed to ensure statistical randomness properties of the bit-stream are encryption-grade. For conventional TRNG designs, a commonly employed post-processing circuit is the Trivium Cipher [21]. The Trivium cipher is a synchronous stream cipher with an internal state of 288-bits represented by $(s_1, \ldots, s_{288})$ and is intended to produce up to 2^{64} key stream bits from an 80-bit secret key and an 80-bit initial value (IV)[23]. A circuit-level implementation of the Trivium cipher can be seen in the inset of Fig. 2 (b). The internal state of the cipher is decomposed into three feedback shift registers (FSRs) and coupled with non-linear feedback combinational logic employing only AND and XOR gates.

In Trivium, two out of three FSRs are loaded with the key and IV, while the remaining bits of the internal state are filled in with a constant value. The cipher state is then executed for $4 \times 288 = 1152$ clock cycles to produce the final bit stream.

C. Simulation Results

Simulation results for the conventional and adaptive TRNG designs are presented in Figs. 3 (a)-(c) and Figs. 3 (d)-(f), respectively. Fig. 3 (a) shows the behavior of the stochastic voltage ($V_{stochastic}$) in the conventional TRNG, while Figs. 3 (b) and (c) show the response of the digitizer voltage ($V_{Digitizer}$) and the random key stream generated after post-processing (with the conventional Trivium cipher implemented using Cryptool 2.1 (Stable Build) [35]), respectively. Fig. 3 (d) shows the behavior

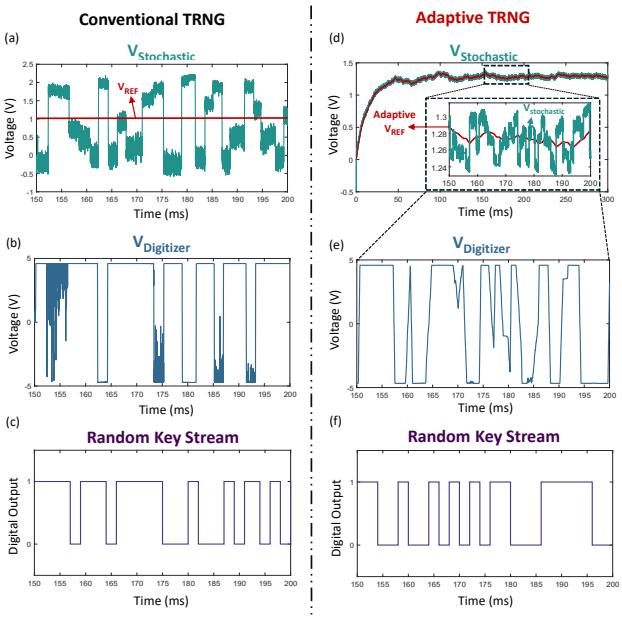

FIG. 3. Simulation results for an sMTJ-based adaptive TRNG. Plots of (a) $V_{Stochastic}$ vs. time, (b) $V_{Digitizer}$ vs. time, and (c) the generated random key stream vs. time, for the conventional TRNG. Plots of (d) $V_{Stochastic}$ vs. time, (e) $V_{Digitizer}$ vs. time and (f) the generated random key stream vs. time, for the adaptive TRNG.

of $V_{stochastic}$ and the adaptive V_{REF} at the output of the low-pass filter in the adaptive TRNG, while Figs. 3 (e) and (f) show the response of $V_{Digitizer}$ and the generated random key stream, respectively. When compared to the conventional TRNG, the proposed adaptive TRNG dynamically tracks $V_{stochastic}$ and tunes itself to adapt to entropy source variations.

Fig. 4 (d) depicts a 2D image of a random key stream generated using the proposed adaptive digitizer after post-processing using a Trivium. The random distribution of white and black pixels indicates an unbiased generation of a random "0/1" bit-stream. The 2D pattern qualitatively demonstrates the uniform distribution of random bits and validates the design's ability to produce an unbiased bit stream with high-quality randomness.

To quantitatively evaluate the randomness qualities of the generated bit stream, statistical randomness tests are conducted. One commonly employed method is using the NIST test suite (NIST SP 800-22), which is a statistical test suite for random and pseudo-random number generators for cryptographic applications [36], and which will be used in the remainder of the presented study. The suite includes 16 tests, the P-value for each test is used as a measure of randomness and is assessed to determine the test's success. A P-value of 1 indicates perfect randomness, while a P-value of 0 indicates no randomness. If the P-value exceeds 0.01, it indicates that the NIST test has been passed successfully.

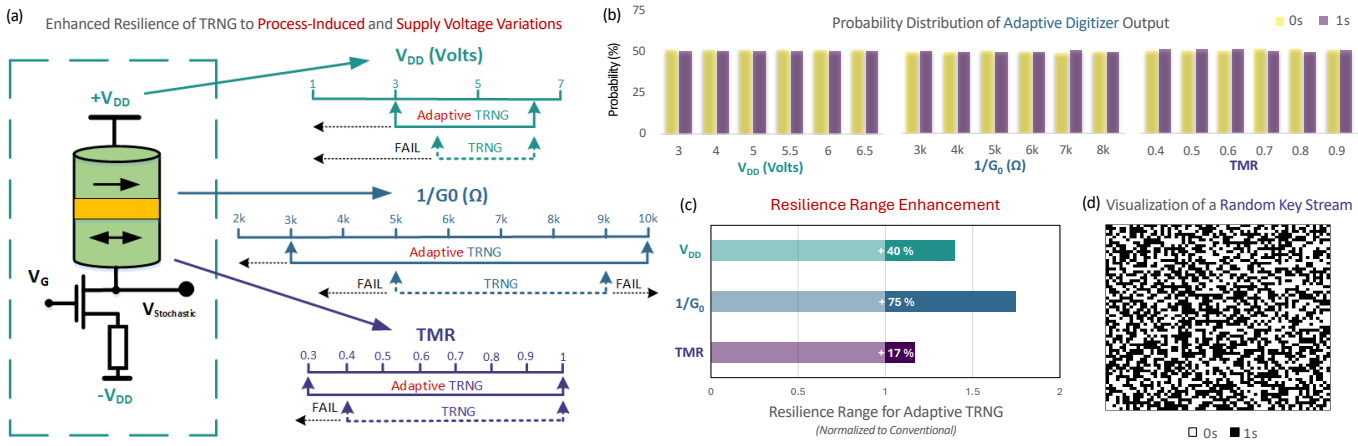

FIG. 4. Process-induced and supply-voltage variation analysis for the proposed adaptive TRNG. (a) Ranges of operation with resilience to variation in V_{DD}, G_0 and TMR. (b) Probability of 1's and 0's for: varying V_{DD}, varying G_0, and varying TMR, from left to right respectively. (c) Resilience range enhancement across the three parameters, V_{DD}, G_0 and TMR, normalized to the resilience range of the conventional design. (d) 2D pattern of a sample generated random bit stream using the presented adaptive TRNG.

D. Adaptive TRNG Variation-Resilience Analysis

In order to investigate the resilience of the adaptive TRNG to variations, simulations of both the conventional and the adaptive TRNG are repeated for a range of process-induced and supply-voltage variations. In addition to supply-voltage variations, the process-induced variations investigated are those that are reflected through variation in two key device parameters: (1) G_0 and (2) TMR. For each case, the simulation was started from a nominal value of the parameter under investigation, then the resulting generated bit stream was tested for randomness using the NIST test suite. For each simulation run a total of 2,398,733 random bits were generated within a period of 0.99 seconds. The adaptive TRNG would be regarded as passing only if the generated bit stream passed all 16 tests. In that case, the obtained p-values were recorded, and then the parameter under test would be incremented with positive increments until it fails by failing at least one test. At that point, the last value where the adaptive TRNG passed all tests would be regarded as the upper limit of the resilience range in that direction. The same procedure would then be repeated in the opposite direction, but with decrements instead of increments, to find the lower limit of the resilience range.

The results of this variation analysis for both the conventional and the proposed adaptive TRNGs are depicted in Fig. 4 (a) through the visually illustrated variation-resilient ranges, where all tests are passed. The detailed results are also shown in Table I. For V_{DD} variation analysis, the starting nominal value was 5 V and then the voltage was incremented in 0.5 V increments until the adaptive TRNG failed at 7.0 V, making 6.5 V as the upper limit of the V_{DD} resilience range. The procedure was repeated again with 0.5 V decrements, leading to a 3.0 V lower limit of the V_{DD} resilience range. The same procedure was also conducted for both G_0 and TMR, and the results are summarized in the visual illustration of Fig. 4 (a). Moreover, the detailed results are also summarized in Table I, with the average P-value for each test, across all scenarios where all the tests were passed, is recorded.

The results of Fig. 4 and Table I demonstrate the enhanced resilience of the adaptive TRNG to variations in V_{DD}, G_0 and TMR compared to a conventional TRNG, reaching up to an enhancement in the variation-resilience range of 40 %, 75 % and 17 %, respectively, as illustrated in Fig. 4 (c). Fig. 4 (b), illustrates the percentage of 1s and 0s for six different cases of varying V_{DD}, G_0, and TMR, respectively. As is evident in all test cases, the percentage of 1s and 0s is close to an ideal 50 % each, thus confirming that the bit patterns are unbiased. Fig. 5 shows a visual illustrative scatter plot of the obtained average P-values from the NIST test suite in the presence of variations, demonstrating that they all fall well within the acceptable range, further highlighting the resilient nature of the adaptive TRNG.

IV. ADAPTIVE RNG WITH A PSEUDO-RANDOM ENTROPY SOURCE

While TRNGs with physically driven naturally random entropy sources provide very high quality true-randomness desired for encryption, the advanced device technologies needed for these TRNGs are not accessible to all IoT device designers, nor are they always applicable in IoT applications that do not justify the high cost of custom designing chips with these technologies. In this section, we show how our adaptive RNG can address this issue by providing a low-cost highly accessible route to embedded encryption in IoT devices. To achieve this, we employ a low-quality pseudo-random entropy source,

TABLE I. Statistical Randomness Test Results Under Process-Induced and Supply Voltage Variations (NIST SP 800-22)

Variation Analysis Parameter	V_{DD} **Variation**			G_0 **Variation**			TMR **Variation**		
Test	Result	P-Value	Pass Rate	Result	P-Value	Pass Rate	Result	P-Value	Pass Rate
Frequency (Monobits)	Pass	0.1721	8/8	Pass	0.6424	8/8	Pass	0.8238	8/8
Frequency within a Block	Pass	0.4658	8/8	Pass	0.1161	8/8	Pass	0.2892	8/8
Runs	Pass	0.4369	8/8	Pass	0.7284	8/8	Pass	0.6554	8/8
Longest Run of Ones in a Block	Pass	0.5977	8/8	Pass	0.3048	8/8	Pass	0.3646	8/8
Binary Matrix Rank	Pass	0.4143	8/8	Pass	0.3638	8/8	Pass	0.3338	8/8
Discrete Fourier Transform (Spectral)	Pass	0.2287	8/8	Pass	0.4369	8/8	Pass	0.7255	8/8
Non-Overlapping Template Matching	Pass	0.6114	8/8	Pass	0.1671	8/8	Pass	0.2771	8/8
Overlapping Template Matching	Pass	0.7457	8/8	Pass	0.3901	8/8	Pass	0.3601	8/8
Maurer's "Universal Statistical"	Pass	0.6514	8/8	Pass	0.5845	8/8	Pass	0.4523	8/8
Linear Complexity	Pass	0.5402	8/8	Pass	0.7001	8/8	Pass	0.1062	8/8
Serial	Pass	0.7153	8/8	Pass	0.0745	8/8	Pass	0.7624	8/8
Approximate Entropy	Pass	0.2519	8/8	Pass	0.3214	8/8	Pass	0.5214	8/8
Cumulative Sums (Forward)	Pass	0.3192	8/8	Pass	0.6984	8/8	Pass	0.6109	8/8
Cumulative Sums (Reverse)	Pass	0.1762	8/8	Pass	0.3647	8/8	Pass	0.5274	8/8
Random Excursions	Pass	0.8595	8/8	Pass	0.7491	8/8	Pass	0.5942	8/8
Random Excursions Variant	Pass	0.5971	8/8	Pass	0.4941	8/8	Pass	0.6424	8/8

an LFSR, which can be viewed as an emulation of the sMTJ but with pseudo randomness. An LFSR is readily implementable on entry-level FPGA prototyping kits, and its design is a well-known text-book design. However, an LFSR on its own does not meet the randomness requirements of encryption, applications. Using our adaptive RNG system, we show how the use of the adaptive digitizer with simplified post-processing can increase the entropy of the LFSR, making it encryption-grade.

A. Enhancing LFSR Randomness with The Adaptive Digitizer

In order to enhance the entropy of the pseudo-random source, the digital output from the LFSR is converted to an analog signal serving as $V_{Stochastic}$, and is then fed into the adaptive digitizer that converts it back to digital. However, here the comparison is against the adaptive moving average - V_{REF} - of this stochastic signal, and hence the generated output bit stream is different than the original bit stream obtained from the LFSR. This output of the adaptive digitizer, will not be the same as the inputted digital bit stream from the LFSR, but will have higher entropy due to the conversion and subsequent adaptive digitization processes that infuses more noise (randomness) into the signal. This output will then undergo post-processing to produce a digital random bit stream with randomness qualities that fulfil the basic requirements of embedded cryptography applications.

B. Compact Post-Processing: The Mini Trivium

Although the Trivium Cipher is regarded as a relatively low area hardware cipher, it still requires thousands of logic gates for implementation and can impose relatively heavy power consumption levels for energy-constrained IoT devices, especially when conducting continuous real-time data encryption; essential in remote sensing. In order to further reduce the required hardware resources for embedded encryption in resource-constrained IoT devices, we also present a modified lower-hardware-cost version of the Trivium cipher used for post-processing, and name it here as a Mini Trivium.

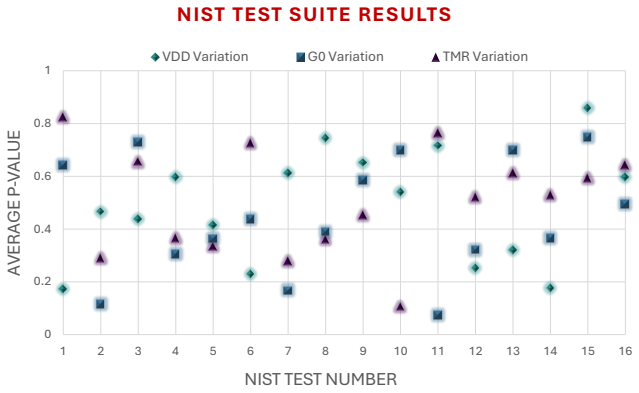

FIG. 5. A scatter plot as a visual illustration of the NIST Test Suite results for the variation analysis. Average P-values across the resilience range to variation in V_{DD}, G_0 and TMR for the adaptive TRNG.

Due to the enhanced randomness qualities of the generated bit stream from the adaptive digitizer, it is possible to achieve adequate post-processing using a circuit with reduced complexity. Accordingly, we employ the simplified Mini Trivium cipher, whose circuit implementation is shown in Fig. 2 (d).

The Mini Trivium circuit simplifies the original Trivium Cipher design by reducing its three Nonlinear Feedback Shift Registers (NFSRs) into a single 19-bit shift register, thus reducing complexity, without compromis-

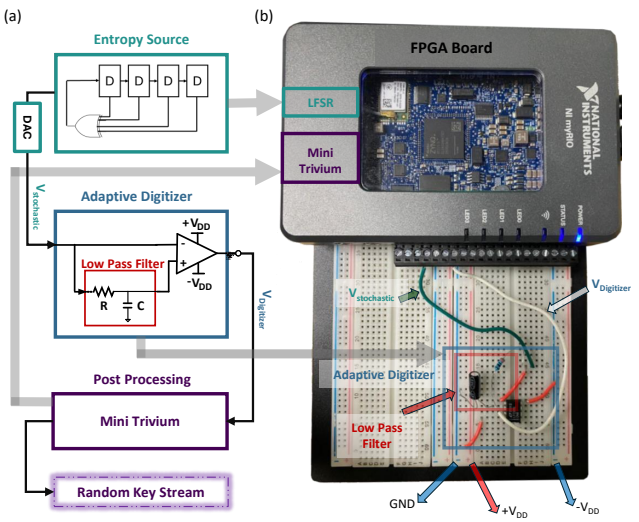

FIG. 6. (a) Schematic diagram of system blocks and interconnections. (b) Experimental implementation of the adaptive RNG system.

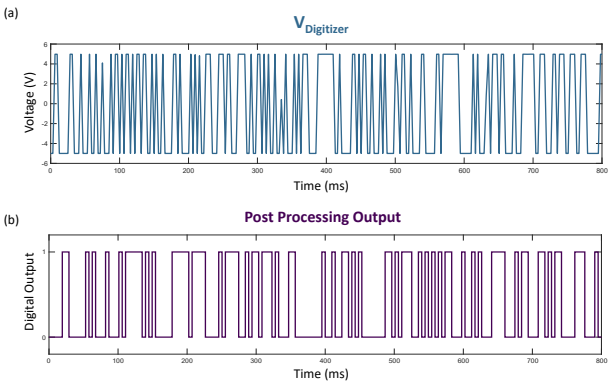

FIG. 7. Measured results from the FPGA experiments, showing (a) the output of the adaptive digitizer and (b) the corresponding generated random bit stream after post-processing with the Mini Trivium.

ing core cryptographic properties. By strategically selecting taps t_1 to t_{10} and reducing core logic gates down to 10 gates only, it achieves faster state updates and key stream generation through streamlined XOR and AND operations. The shorter register length and reduced feedback paths enable quicker initialization cycles compared to Trivium's 288-bit state. Despite fewer bits, non-linearity is preserved via carefully placed gates, balancing security and efficiency.

C. Experimental Implementation and Results

To test the overall proposed adaptive RNG system with the LFSR and the Mini-Trivium, the design was experimentally implemented using an FPGA board (NI myRIO-1900), as depicted in Fig. 6 (b). The schematic of Fig. 6 (a) depicts the complete system implementation, showing the connections between various components of the system. The combination of the linear feedback shift register (LFSR) along with the digital-to-analog converter (DAC) is employed as the entropy source that generates an analog stochastic signal ($V_{Stochastic}$), similar to the signal produced by the sMTJ and its associated circuitry presented in the previous section. Once generated, $V_{Stochastic}$ is then fed into both the LPF and and the comparator analog circuits within the adaptive digitizer. The LPF and the comparator of the adaptive digitizer were implemented using off-the-shelf discrete components on a breadboard, nonetheless, they can also be implemented using integrated components.

A sample output from the adaptive digitizer is shown in Fig. 7 (a). As shown in the figure, the output looks like a non-ideal digital signal with finite slopes, and this is due to the limited slew rate (SR) of the used operational amplifier (OpAmp) for the comparator [37]. To obtain more ideal digital waveforms, a comparator with a higher SR can be employed or designed. This output from the adaptive digitizer - obtained using the breadboard-implemented analog circuit shown in Fig. 6 (b) - is then passed through the Mini Trivium cipher for post-processing. Fig. 7 (b) shows the generated random bit stream from the adaptive digitizer output of Fig. 7 (a) after post-processing. The compact Mini Trivium post-processing circuit was implemented using the FPGA unit. The FPGA unit was programmed and tested using a LABVIEW environment.

In order to investigate the enhancement that the adaptive RNG system provides to the raw LFSR entropy source, when running any experiment both: (1) the raw bit stream generated by the LFSR only, and (2) the final generated random bit stream after the adaptive digitizer and post-processing were recorded. The system was operated to generate a random bit stream of 1,670,000 bits in each experiment. This run was repeated 10 independent times providing 10 independent experiments. Each time the experiment was conducted, the generated raw random bit stream from the LFSR only and the final random bit stream generated by the adaptive RNG were each tested individually using the NIST test suite for randomness. A similar set of simulation runs were also conducted on the sMTJ-based adaptive TRNG system for comparison purposes. The results for all three systems: (1) LFSR only, (2) LFSR-based adapative RNG, and (3) sMTJ-based adaptive TRNG are summarized in Table II. Moreover, the results for the average P-values for each individual NIST test for all the three systems, are presented visually through the scatter plot of Fig. 8.

As the results of Table II show, the LFSR on its own fails 12 out 16 tests consistently in all 10 experiments, confirming that the LFSR on its own is a low-quality PRNG. On the other hand, when the same random bit stream generated by the LFSR goes through the adaptive RNG system, namely the DAC, adaptive digitizer

TABLE II. Comparison Between Different RNG Types (NIST SP 800-22 Test Suite)

System Under Test	LFSR ONLY*			Adaptive RNG (LFSR)**			Adaptive TRNG (sMTJ)***		
Test	Result	P-Value	Pass Rate	Result	P-Value	Pass Rate	Result	P-Value	Pass Rate
Frequency (Monobits)	Fail	0.000	0/10	Pass	0.414	10/10	Pass	0.799	10/10
Frequency within a Block	Fail	0.000	0/10	Pass	0.479	10/10	Pass	0.851	10/10
Runs	Fail	0.000	0/10	Pass	0.728	10/10	Pass	0.961	10/10
Longest Run of Ones in a Block	Fail	0.000	0/10	Pass	0.946	10/10	Pass	0.727	10/10
Binary Matrix Rank	Fail	0.000	0/10	Pass	0.881	10/10	Pass	0.333	10/10
Discrete Fourier Transform (Spectral)	Fail	0.000	0/10	Pass	0.223	10/10	Pass	0.569	10/10
Non-Overlapping Template Matching	Fail	0.000	0/10	Pass	0.274	10/10	Pass	0.619	10/10
Overlapping Template Matching	Fail	0.000	0/10	Pass	0.219	10/10	Pass	0.662	10/10
Maurer's "Universal Statistical"	Fail	0.000	0/10	Pass	0.434	10/10	Pass	0.551	10/10
Linear Complexity	Fail	0.000	0/10	Pass	0.754	10/10	Pass	0.314	10/10
Serial	Fail	0.000	0/10	Pass	0.831	10/10	Pass	0.381	10/10
Approximate Entropy	Fail	0.000	0/10	Pass	0.556	10/10	Pass	0.445	10/10
Cumulative Sums (Forward)	Pass	1.000	10/10	Pass	0.782	10/10	Pass	0.652	10/10
Cumulative Sums (Reverse)	Pass	1.000	10/10	Pass	0.309	10/10	Pass	0.625	10/10
Random Excursions	Pass	0.849	10/10	Pass	0.521	10/10	Pass	0.885	10/10
Random Excursions Variant	Pass	0.617	10/10	Pass	0.778	10/10	Pass	0.629	10/10

*Experiment: entropy source: LFSR.

**Experiment: entropy source: LFSR + DAC, post-processing: Mini Trivium.

***Simulation: entropy source: sMTJ and associated circuitry, post-processing: Trivium.

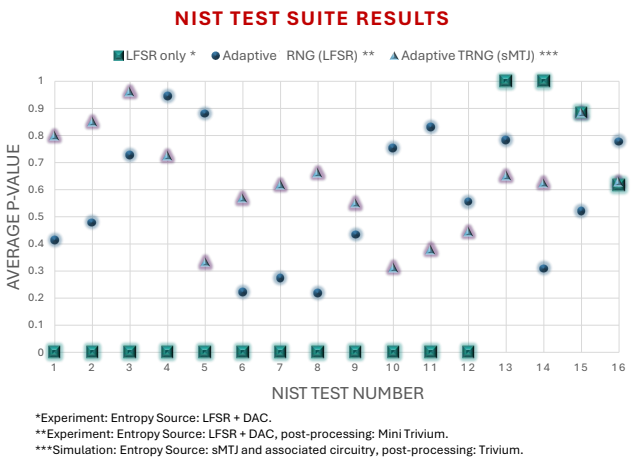

FIG. 8. NIST Test Suite results comparing a conventional LFSR with both an LFSR-based adaptive RNG and an sMTJ-based adaptive TRNG

and the Mini Trivium cipher, then the resulting random bit stream shows excellent statistical randomness properties, consistently passing all 16 tests during all conducted experiments. Not only do the random bit streams from the LFSR-based adaptive RNG pass the tests, but they do so with excellent p-values consistently above 0.2. The obtained P-values are indeed comparable to the results obtained for the sMTJ-based adaptive TRNG system at nominal conditions, as shown quantitatively through both Table II and the visual illustration of Fig. 8. The experimental results confirm that the LFSR-based adaptive RNG implementation using off-the-shelf components results in the generation of high quality random numbers with properties suitable for embedded encryption.

V. CONCLUSION

In this work, we demonstrated an adaptive RNG for variation-resilient extraction of random numbers from entropy sources based on emerging device technologies. Two demonstrations were presented, one employing an sMTJ-based entropy source, which was comprehensively evaluated using MATLAB + SPICE simulations, and the other employing an LFSR-based pseudo random entropy source that emulates the true-random source, which was experimentally implemented using an FPGA.

A key component of the adaptive RNG system was its adaptive digitizer, which employed a low-pass filter to generate an adaptive reference voltage that tracks any deviation or drift in the generated stochastic signal from the entropy source, enabling variation-resilience and allowing extraction of unbiased random bit streams with high entropy. Statistical properties of generated bit streams by the adaptive RNGs were tested using the NIST test suite, demonstrating encryption-grade randomness consistently. The presented adaptive RNG has great potential for use in embedded encryption within IoT devices, making data encryption accessible locally.

ACKNOWLEDGMENT

Authors thank Mahmood A. Mohammed for feedback. Part of the work of F. Zahoor and F. Al-Dirini was done at KFUPM. Authors acknowledge support of the Natural Sciences and Engineering Research Council of Canada (NSERC) [Grant number: RGPIN-2023-03743], and partial support of KFUPM [Grant number: INAM2306].

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