Bias Variation Compensation in Perimeter-Gated SPAD TRNGs

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Abstract—Random number generators that utilize arrays of entropy source elements suffer from bias variation (BV). Despite the availability of efficient debiasing algorithms, optimized implementations of hardware friendly options depend on the bit bias in the raw bit streams and cannot accommodate a wide BV. In this work, we present a 64 × 64 array of perimeter gated single photon avalanche diodes (pgSPADs), fabricated in a 0.35 μ m standard CMOS technology, as a source of entropy to generate random binary strings with a BV compensation technique. By applying proper gate voltages based on the devices' native dark count rates, we demonstrate less than 1% BV for a raw-bit generation rate of 2 kHz/pixel at room temperature. The raw bits were debiased using the classical iterative Von Neumann's algorithm and the debiased bits were found to pass all of the 16 tests from NIST's Statistical Test Suite.

Index Terms—Debiasing, iterative Von Neumann, dark count rate, NIST STS, pgSPAD, perimeter gating

I. INTRODUCTION

Random number generators (RNGs) find applications in various domains such as cryptography, gaming, scientific research, computer simulations, and machine learning [1]–[3]. In secure communication systems, they are an indispensable building block for generating nonces and session keys [4]. Depending on the application's need, they can be implemented using natural sources of randomness, *i.e.*, as true RNGs (TRNGs) [5], [6] or using complex, yet deterministic algorithms, *i.e.*, as pseudo-RNGs (PRNGs) [7], [8]. However, TRNGs are preferred over PRNGs when unpredictability is of the utmost concern [9].

As shown in Fig. 1, a TRNG requires a physical entropy source, which is sampled for its fluctuating random states over time by a bit extraction mechanism [10]. Depending on the extraction criteria, the raw bits may require post-processing by one or more debiasing stages in order to increase the entropy in the output bit-streams [11], [12].

TRNGs can be constructed using any classical source of noise, such as the thermal noise of resistors [13]. However, quantum RNGs (QRNGs) are superior in terms of security, which leverage quantum randomness [14]. For example, the uncertainty pertaining to photon statistics can be utilized to



Fig. 1. Basic building blocks of a TRNG including an entropy source fluctuating between random states at an average rate of r_s . The states are sampled periodically (r_{clk}) to generate one or more bits (r_b) depending on the bit extraction method. The raw bit sequences may need to be debiased to generate one or more processed bit-streams (*i.e.*, r_{VN} , r_{XOR} , r_{RES}). Example is shown for the iterative Von Neumann (IVN) debiasing algorithm.

generate quantum random numbers [15]–[17]. As such, single photon avalanche diodes (SPADs) are commonly found to be the photon transducers in photon-based QRNGs.

SPADs are p-n junction diodes that are operated beyond their nominal reverse breakdown voltage; this operational regime is commonly known as the Geiger mode. The resulting high electric field at the depleted junction makes the devices sensitive enough to detect individual incident photons. An electron-hole pair generated from photon absorption can probabilistically initiate an avalanche event which can be time-tagged by an external sensing circuit *i.e.*, using a timeto-digital converter (TDC) [17], [18]. Similarly, the number of avalanche events within a defined time window can be accumulated by integration [19], [20]. Random bits can be generated from these random detection times or random amounts of detected events.

SPAD arrays provide increased throughput. They are usually coupled to a photon source attenuated with neutral density filters [21]. The latter feature increases hardware overhead. These systems are also limited by the nonuniform illumination from the photon source leading to bias variation across the array. Moreover, device manufacturing variation can further cause bias variation, posing non-trivial challenges [22], [23].

An alternative to the photon-based systems is SPAD dark noise-based TRNGs [24], [25]. Recently, we have demonstrated a perimeter gated SPAD (pgSPAD) dark noise-based TRNG with near zero bias and temperature stability [26]. This variant of SPADs utilizes a polysilicon gate over the perimeter junction to modulate the dark carrier generation rate [27]. In this work, we extend our study to analyze the behavior of a pgSPAD array in terms of its native BV and the underlying trade-offs with bit generation rate. In particular, we show that hardware-friendly algorithms like iterative Von

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Fig. 2. A pgSPAD die-on-PCB prototype board (a) with the digital (control & data) and the analog (power & tuner) ports. The 5 $mm \times 5 mm$ die (b) contains a 64 × 64 pgSPAD pixel array, surrounded by the peripheral control blocks for pixel selection, active quench & reset, and data readout. Inset shows a photo-micrograph of the 50 $\mu m \times 50 \mu m$ pixels, each containing a pgSPAD and its sensing circuitry. In-depth circuit details can be found in Ref. [27].



Fig. 3. Simplified schematic of the dark count based TRNG using a perimeter gated SPAD (a). Analog voltage of the cathode (V_C) is digitized at the inverter's output (V_o) which triggers the active quench and reset, and the counter blocks. The dark count probability (P_{DC}) can be altered by the perimeter gate voltage (V_G) , generating bit-steams with different biases (b).

Neumann (IVN) debiasing [28] can benefit from BV reduction using perimeter gating, which obviates the need for custom optimization.

II. PGSPAD ARRAY: THE ENTROPY SOURCE

Figure 2 (a) shows a prototype die-on-PCB with a 5 $mm \times$ 5 mm pgSPAD array fabricated in a 0.35 μm standard CMOS process. A photomicrograph (Fig. 2 (b)) of the die shows the 64 × 64 pixel array, surrounded by the control logic blocks. The pixel architecture, consisting of a diode and its sensing circuitry, is shown in the inset. In-depth circuit details and operational characteristics of the device can be found in ref. [27]. Nevertheless, we briefly describe the operation of the device below.

Figure 3 (a) shows a simplified schematic of a generic pixel. When a particular pixel is selected, a precharge (*PRE*) signal pulls the cathode voltage, V_C to V_{DD} while the counter gets reset. By de-asserting *PRE*, the device is allowed to be triggered by photo- or dark-carriers while being actively quenched to V_Q and reset to V_R in a free-running mode. Specifically in the dark, the average triggering rate, λ_0 , also known as the dark count rate (DCR) is proportional to the dark carrier generation rate, dominated by thermal excitation, trap assisted tunneling, and band-to-band tunneling (B2B) [29].



Fig. 4. Conventional bit generation protocols from interdetection times and the number of detected events (a). Zero bias condition can be achieved (b) for equal probability of $N_i = 0$ and $N_i \neq 0$ by maintaining $\lambda T = ln(2)$.

B2B, and consequently the DCR, can be modulated by the excess bias voltage, $V_{ex} = (V_R - V_A) - V_{brk}$ and the perimeter gate voltage, V_G . Here, V_A is the applied anode voltage and V_{brk} is the diode's breakdown voltage.

Considering afterpulsing and deadtime, the probability of observing a dark event (P_{DC}) within T_{int} is expressed as

$$P_{DC} = 1 - e^{-\lambda_{eff} T_{int}} \tag{1}$$

where,

$$\lambda_{eff} = \frac{\lambda_0}{1 - \tilde{p}_a + \lambda_0 (\tau_R / T_{int})}.$$
(2)

Here, \tilde{p}_a is the adjusted afterpulsing probability, and τ_R is the adjusted device recovery time taking quenching and probabilistic reset time into consideration [30].

Figure 3 (b) shows the time-series of the LSB flip of the counter as P_{DC} is varied via the gate voltage (V_G). Each spike denotes a dark event detection. As V_G increases, the probability of a dark event detection decreases [26].

III. RANDOM BIT EXTRACTION PROTOCOL

Comparison between the inter-detection times Δt_i 's (see Fig. 4 (a)) usually involves power-consuming TDCs. An energy-efficient alternative to this is the counter-based approach to track the number of detected events, N_i 's in each fixed time-window, Tw_i . By properly adjusting the activity rate, λ and the window duration, T, it is possible to operate the device at zero bias with equal probability of N = 0 and $N \neq 0$ (see Fig. 4 (b)). Specifically, it only requires that

$$\lambda T = ln(2). \tag{3}$$

With bias, b defined as $b = \frac{|p_1-p_0|}{2} = \frac{|P_{DC}-(1-P_{DC})|}{2}$, where p_1 and p_0 are the probabilities of N = 0 and $N \neq 0$, respectively, Eqs. 1 and 3 ensure that $b \rightarrow 0$ for different combinations of dark activities and integration times.

However, T is defined and fixed for all pixels in an array by the bit-sampling rate. Hence, the intrinsic variation of λ leads to a pixel-wise bias resulting in

$$b_i = |0.5 - e^{-\lambda_{eff,i} T_{int}}| \times 100\%.$$
(4)



Fig. 5. Classical implementation of IVN [28] (a) with 7 elements. Throughput distribution and variation with respect to the bias in the input string (b). More than a 12% bias reduces the total throughput by more than 5%.

A higher degree of bias degrades the overall entropy of the output. Therefore, as a standard practice, the raw bits are post processed by debiasing stages such as the IVN algorithm to restore the entropy in the output streams.

IV. DEBIASING METHOD: ITERATIVE VN ALGORITHM

Von Neumann (VN) post processing is a hardware-friendly method, famous for debiasing raw bit sequences in a resourceconstrained setup [31]. While this method guarantees full entropy recovery, provided that the bits are independent, it loses a substantial amount of bits in the process [15].

Table I shows the bit assignment rules for the VN process. The raw bits in a sequence, S are paired up to create S_{PAIR} which are either discarded or replaced by a 0 or a 1 depending on the pair combinations shown in the $S_{PAIR} \rightarrow S_{VN}$ transformation. This results in a 75% reduction in the throughput at the very least depending on the bias in the input string [28].

To increase the throughput, an iterative VN (IVN) process was proposed by Peres with the idea of re-applying VN on the discarded information [32]. In theory, it is possible to extract the maximum entropy available from the original bit sequence by iterating the IVN procedure to infinity on the resulting XOR sequence, S_{XOR} and the residual sequence, S_{RES} after each iteration according to the rules shown in Table I [28].

However, due to area and energy constraints, a finite number of stages are utilized as shown by the block diagram in Fig. 5 (a) depicting a classical IVN implementation. Since each stage takes up the same area and power for a rapidly diminishing throughput as shown in Fig. 5 (b), a procedure to optimize the connection-tree for a given number of stages was proposed in Ref. [28]. However, such optimization methods depend on the bias, b in the raw input since both the throughput and the



Fig. 6. DCR distribution (a) at room temperature for an excess bias of $\sim 2 V$ and a perimeter gate voltage of 0 V. Exponential decrease of individual DCR with the increase of the gate voltage magnitude (b). Spatial distribution (c) and the histogram (d) of bias for 0 V on the gate with $T = ln(2)/\bar{\lambda_0} \sim 50 \ \mu s$.

bias propagation directly depend on it (see Table I and Fig. 5 (b)). Additionally, it is impractical to implement a custom optimized connection-tree for each TRNG unit in an array to accommodate a wide bias variation (BV) [23].

V. EXPERIMENTAL RESULTS AND DISCUSSIONS

A. Native DCR and the Bias Variation Across the Array

Figure 6 (a) shows the DCR histogram for 4,096 pixels operating at room temperature with $V_{ex} \sim 2 V$ and $V_G =$ 0 V. We see a DCR range of $\sim 35 \ kHz$ with an average, $\overline{\lambda_0} \sim 14 \ kHz$. Figure 6 (b) shows the exponential decrease of the DCR across the entire array with the increase of the perimeter gate voltage magnitude. Here, we have presented the fitted trend lines for 100 randomly selected pixels, including the most active and the least active ones. We can empirically express the DCR, λ_i of a unit as the function of $V_{G,i}$ as

$$\lambda_i(V_G) = \lambda_{0,i} e^{-\alpha_i V_{G,i}} \tag{5}$$

where, $\alpha_i(V^{-1})$ is the gate voltage coefficient of the exponent.

Therefore, it is possible to apply pixel-specific optimal gate voltage $V_{G,i}^*$ to make the array exhibit the same DCR, *i.e.*, $ln(2)/T_0$ (shown by the red broken line) by all the pixels. Here, T_0 is the sampling time for a 0 bias variation.

Figures 6 (c) and (d) show the spatial distribution and the histogram of the native bias of the array, respectively, for $V_G = 0 V$ and $T = ln(2)/\bar{\lambda_0} \sim 50 \ \mu s$. This corresponds to a raw bit generation rate of $20 \ kHz/pixel$. The array average bias was found to be $\sim 14\%$ with a BV $\sim 9\%$, calculated as the standard deviation of the bias across the array.

B. Bias Variation Compensation with Perimeter Gating

By increasing the gate voltage magnitude, it is possible to reduce the dark activity of each pixel to a desired level



Fig. 7. Reduction of average bias from 14% to 8% by applying appropriate gate voltages to pixels exhibiting higher than the native average DCR (a). Relationship of the average bias and the bias variation with the bit-sampling time (b) showing the trade-off between bias and bit-generation rate. We found $T = 0.5 \ ms$ corresponding to a BV < 1%.

(see Fig. 6 (b)). However, pixels exhibiting DCRs below that desired activity level will still contribute to the bias variation. Therefore, it is necessary to select a DCR activity level that is close to the array minimum to achieve a ~ 0 BV.

For instance, Fig. 7 (a) shows the histogram and the spatial variation (inset) of the bias as we reduce the activity of the pixels exhibiting higher DCR than the native average, $\overline{\lambda_0} = 14 \ kHz$ by applying appropriate gate voltages. Although this reduced the array average bias, b_{avg} to ~ 8% from its native value of ~ 14%, BV is still ~ 9% since 50% of the pixels have lower dark count activity than the one required to satisfy $\lambda T = ln(2)$ for $T = 50 \ \mu s$. Therefore, to reduce the required λ , we needed to increase the sampling time, T.

Figure. 7 (b) shows the b_{avg} and the BV as we swept the sampling time from 0.1 ms to 1 ms. For each value of T, the gate voltages were adjusted to confine the dark noise activity of individual pixels close to the required value, *i.e.*, ln(2)/T.

Hence, we readily see the trade-off between the sampling time or bit-generation rate with the BV as both the average bias and the bias variation decrease as we increase the sampling time. In other words, a lower bit generation rate allows for a lower average bias and a near zero BV. Consequently, we selected a raw bit-generation rate of 2 kHz/pixel to achieve a BV less than 1% to use the classical IVN connection-tree without needing any optimization. However, it should be noted that higher bit-generation rates can be accommodated while incurring a greater BV if optimized IVN connection-trees with more stages are deployed [28].

C. Bit-Streams Generation and Testing with the NIST STS

We generated random bits from random pixels across the array with the target maximum BV of < 1%. Each of the raw bits were debiased using a 3-stage classical IVN algorithm to obtain > 1M bits/string. The resulting bit strings were tested using the 16 statistical tests prescribed by NIST [33].

We have created a MATLAB based GUI for the NIST Statistical Test Suite (STS) as a part of this work, which is easy to use and flexible on the input data file type. Fig. 8 (a) shows the GUI with the results of a random bit string passing all the tests similar to the rest of the debiased bit-strings.



Fig. 8. MATLAB GUI [34] created to test the quality of the debiased bitstrings (a) and the p-value bar plots (b) by administering the 16 statistical tests prescribed by NIST [33].

Fig. 8 (b) shows the tests that were performed along with the p-value ranges obtained from the tests. Here, randomness is confirmed when a p-value is greater than the confidence level of a test, which we set to the default value of $\alpha = 0.01$.

All tests were performed with the default setup prescribed by NIST. Furthermore, we note that for the random excursions and random excursions variant tests, we considered the minimum of the possible 8 and 18 p-values, respectively, to conclude a pass or fail for the given string.

VI. CONCLUSIONS

In this work, we have presented the utility of the perimeter gating technique to reduce the bias variation (BV) in a true random number generator (TRNG) implemented with a single photon avalanche diode (SPAD) array. Our dark noise-based approach eliminates the need for bulky optical components such as a light source, neutral density filter, lenses, and diffusers. By keeping the BV less than 1%, we were able to use the classical iterative Von Neumann debiasing without needing to implement any custom optimization for the connection-tree on a pixel-by-pixel basis. This proposed pgSPAD TRNG array can be easily integrated in an areaconstrained application, such as low-power remote IoT devices needing frequent authentication to establish secure communication links. Furthermore, the TRNG can be augmented by any pseudo-RNG to increase the bit-generation rate impacted by lower BV operating conditions. For larger array formats, sub-arrays can share the the perimeter gate control voltage.

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